METHODS OF FORMING METALLURGY STRUCTURES FOR WIRE AND SOLDER BONDING AND RELATED STRUCTURES

BACKGROUND OF THE INVENTION

The present invention relates to the field of integrated circuits and more particularly to interconnections of integrated circuit devices and related methods and structures.

High performance microelectronic devices often use solder balls or solder bumps for electrical interconnection to other microelectronic devices. For example, a very large scale integration (VLSI) chip may be electrically connected to a circuit board or other next level packaging substrate using solder balls or solder bumps. This connection technology is also referred to as "Controlled Collapse Chip Connection--C4" or "flip-chip" technology, and will be referred to herein as solder bumps.

According to solder bump technology developed by IBM, solder bumps are formed by evaporation through openings in a shadow mask which is clamped to an integrated circuit wafer. For example, U.S. Pat. No. 5,234,149 entitled "Debondable Metallic Bonding Method" to Katz et al. discloses an electronic device with chip wiring terminals and metallization layers. The wiring terminals are typically essentially aluminum, and the metallization layers may include a titanium or chromium localized adhesive layer, a co-deposited localized chromium copper layer, a localized wettable copper layer, and a localized gold or tin capping layer. An evaporated localized lead-tin solder layer is located on the capping layer.

Solder bump technology based on an electroplating method has also been actively pursued. The electroplating method is particularly useful for larger substrates and smaller bumps. In this method, an "under bump metallurgy" (UBM) layer is deposited on a microelectronic substrate having contact pads thereon, typically by evaporation or sputtering. A continuous under bump metallurgy layer is typically provided on the pads and on the substrate between the pads, in order to allow current flow during solder plating.

An example of an electroplating method with an under bump metallurgy layer is discussed in U.S. Pat. No. 5,162,257 entitled "Solder Bump

Fabrication Method" to Yung and assigned to the assignee of the present application. In this patent, the under bump metallurgy layer includes a chromium layer adjacent the substrate and pads, a top copper layer which acts as a solderable metal, and a phased chromium/copper layer between the chromium and copper layers. The base of the solder bump is preserved by converting the under bump metallurgy layer between the solder bump and contact pad into an intermetallic of the solder and the solderable component of the under bump metallurgy layer.

SUMMARY OF THE INVENTION

According to aspects of the present invention, metallurgy structures can be provided for input/output pads of an electronic device comprising a substrate, and first and second input/output pads on the substrate. In particular, first and second metallurgy structures can be provided on the respective first and second input/output pads, with the first and second metallurgy structures having a shared metallurgy structure adapted to receive solder and wire bonds. The metallurgy structures can thus be formed efficiently at the same time to facilitate solder bonding to another substrate and wire bonding to a next level packaging structure.

According to additional aspects of the present invention, metallurgy structures according to the present invention can include an underbump metallurgy layer on an input/output pad, a barrier layer on the underbump metallurgy layer, and a passivation layer on the barrier layer. Such a structure can accept either a wire bond or a solder bond.

According to further aspects of the present invention, an electronic device can include a substrate, an input/output pad on the substrate, and a bonding structure on the input/output pad. More particularly, the bonding structure can include a barrier layer comprising nickel on the input/output pad, and a solder structure on the barrier layer.

According to yet further aspects of the present invention, first and second barrier layers can be provided on the respective first and second input/output pads wherein the first and second barrier layers each comprise nickel. First and second passivation layers can be provided on the respective first and second barrier layers, and a solder structure can be provided on the

first passivation layer while maintaining the second passivation layer free of solder.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-C are cross sectional views illustrating intermediate operations of forming metallurgy structures for input/output pads according to embodiments of the present invention.

Figures 2A-C are cross sectional views illustrating intermediate operations and structures of bonding a second substrate according to embodiments of the present invention.

Figures 3A-B are cross sectional views illustrating alternate intermediate operations and structures of bonding a second substrate according to embodiments of the present invention.

Figure 4 is a plan view of a substrate including metallurgy structures according to the present invention.

Figure 5 is a plan view of a "flip chip" to be bonded to the substrate of Figure 4.

Figure 6 is a plan view of the "flip chip" of Figure 5 bonded to the substrate of Figure 4.

DETAILED DESCRIPTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Also, when an element is referred to as being

"bonded" to another element, it can be directly bonded to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly bonded" to another element, there are no intervening elements present.

According to embodiments of the present invention, a shared metallurgy structure can be used to provide both solder bonding and wire bonding for input/output pads. The same fabrication operations can, thus, be used to provide metallurgy on a first input/output pad of a first integrated circuit device for a solder bond and to provide metallurgy on a second input/output pad of the first integrated circuit device for a wire bond. A second integrated circuit device can thus be solder bonded to one or more input/output pads of the first integrated circuit device, and wires can be bonded to one or more other input/output pads of the integrated circuit device without forming different metallurgies for the solder and wire bonds.

Operations of forming metallurgies for solder and wire bonds are illustrated, by way of example, in Figures 1A-C. As shown in Figure 1A, the integrated circuit device may include a substrate **21**, a plurality of input/output pads **23a-d**, and a protective insulating layer **25**. As will be understood by one of skill in the art, the integrated circuit device may include a plurality of electronic devices formed in/on a semiconductor portion of the substrate **21** with electrical coupling provided with the input/output pads **23a-d**. Moreover, the protective insulating layer **25** may be considered a part of the substrate **21**. While the protective insulating layer **25** is shown on the input/output pads with portions of the input/output pads being exposed thereby, the input/output pads may be formed on the protective insulating layer, or the integrated circuit device may be provided without a protective insulating layer. The input/output pads may comprise aluminum, copper, or other pad materials known to those having skill in the art.

The integrated circuit device including the substrate, input/output pads, and the protective insulating layer, for example, may be fabricated at a first location, and then shipped to a second packaging facility to provide metallurgy structures according to the present invention. Alternately, metallurgy structures may be provided in the same facility used to fabricate the

integrated circuit device including the substrate, the input/output pads, and the protective insulating layer.

As shown in Figure 1A, an under bump metallurgy layer **27** can be formed to provide adhesion to the input/output pads **23a-d**, and/or to provide conduction for subsequent electroplating. The under bump metallurgy layer **27**, for example, can include a first adhesion layer of a material such as titanium, tantalum, tantalum nitride, titanium tungsten, and/or titanium nitride on the input/output pads, and a second conduction layer of a material such as copper and/or gold on the adhesion layer. Alternately, separate adhesion and conduction layers may not be needed if a single layer provides sufficient adhesion and/or conduction. The under bump metallurgy layer may be formed by sputtering, evaporation, or any other techniques known to those having skill in the art. Under bump metallurgy layers are further discussed, for example, in U.S. Patent No. 6,222,279 to Mis et al. entitled "Solder Bump Fabrication Methods And Structures Including A Titanium Barrier Layer", the disclosure of which is hereby incorporated herein in its entirety by reference. The '279 patent is assigned to the assignee of the present invention, and the '279 patent and the present invention share common inventors.

Prior to forming the under bump metallurgy layer, it may be desirable to treat exposed input/output pad **23a-d** surfaces to remove surface oxides and/or contamination that might increase contact resistance between the under bump metallurgy layer and the input/output pads. For example, one or more surface treatments such as a wet chemical dip, a sputtering process, and/or a dry etch may be preformed.

A patterned masking layer **29**, such as a photoresist layer, can then be formed on the under bump metallurgy layer **27** so that subsequent portions of the metallurgy can be selectively electroplated. The patterned masking layer, for example, may be an organic material such as a spun on resist or a dry film patterned using known photolithographic techniques. Barrier layers **31a-d** and passivation layers **33a-d** can then be formed by electroplating on portions of the under bump metallurgy layer exposed by the masking layer **29**. The barrier layers, for example, can be layers of a material such as nickel, platinum, and/or palladium that can reduce solder diffusion. The passivation layers, for example, can be layers of gold, gold-tin, copper, and/or aluminum

that can reduce oxidation of the barrier layer, that can provide a solder wettable surface and that can provide a suitable wire bonding surface. According to particular embodiments, the barrier layers **31a-d** can have thicknesses in the range of 0.5 to 2.0 microns, and passivation layers **33a-d** can have thicknesses in the range of 0.05 to 2.0 microns. For example, a gold passivation layer having a thickness in the range of 0.05 microns to 2.0 microns can provide a solder wettable surface that is suitable for solder bonding and a surface that is also suitable for wire bonding.

As shown in Figure 1B, the masking layer **29** can be removed thereby exposing portions of the under bump metallurgy layer. The exposed portions of the under bump metallurgy layer can then be removed as shown in Figure 1C. The barrier layers and/or passivation layers, for example, can be used as a mask to selectively etch exposed portions of the under bump metallurgy layer. According to particular embodiments, for example, gold passivation layers and nickel barrier layers can be used to mask the under bump metallurgy layer wherein a copper portion of the under bump metallurgy is removed using a NH_4OH/H_2O_2 etchant and a titanium portion of the under bump metallurgy layer is removed using a buffered fluoride etch. Alternately, an additional masking layer can be used for the selective removal of the exposed portions of the under bump metallurgy layer.

As shown in Figure 1C, the resulting metallurgy structures **34a-d** include respective under bump metallurgy layers **27a-d**, barrier layers **31a-d**, and passivation layers **33a-d**. Each of these metallurgy structures may be used for solder or wire bonding as discussed in greater detail below. To the best of their knowledge, the inventors are the first to realize that a shared metallurgy structure can be used for solder and wire bonding. Accordingly, the same fabrication operations can be efficiently used to provide metallurgy structures for input/output pads to provide subsequent wire and solder bonding. While an example of such a metallurgy structure is illustrated in Figure 1C, other metallurgy structures adapted to receive both wire and solder bonds are contemplated according to the present invention.

Moreover, while an example of a method of forming the structure of Figure 1C is illustrated in Figures 1A-C, other methods could alternately be used to provide the structure of Figure 1C. For example, continuous under

bump metallurgy, barrier, and passivation layers could be formed on the substrate including the input/output pads and then selectively etched using photolithographic techniques. The continuous under bump metallurgy, barrier, and passivation layers could be formed using any known deposition techniques such as evaporation, sputtering, electroplating, or combinations thereof. If a technique other than electroplating is used, an under bump metallurgy layer may be provided without a separate conduction layer included therein.

As further shown in the structure of Figure 1C, the metallurgy structures **34a-d** can provide for solder or wire bonding adjacent the respective input/output pads **23a-d**. Alternately, metallurgy structures according to the present invention could provide for solder or wire bonding remote from the respective input/output pad with electrical coupling and redistribution thereto. Redistribution routing conductors are discussed, for example, in U.S. Patent No. 5,892,179 entitled "Solder bumps and structures for integrated redistribution routing conductors" to Rinne et al., the disclosure of which is hereby incorporated herein in its entirety by reference. In addition, it is noted that U.S. Patent No. 5,892,179 and the present invention are commonly assigned and U.S. Patent No. 5,892,179 share a common inventor.

Examples of operations of providing wire and solder bonds to a structure according to Figure 1C are illustrated in Figures 2A-C. Prior to forming wire and/or solder bonds, it may be useful to flux the exposed surfaces of the passivation layers. As shown in Figure 2A, solder balls may be applied to one or more of the metallurgy structures **34a'-d'** where solder bonds are to be applied. For example, preformed solder structures **35b'-c'** (such as solder balls) may be placed on metallurgy structures **34b'** and **34c'** manually or using automated placement tools. Alternately, solder structures could be electroplated, evaporated, or otherwise provided on the metallurgy structures. With the structure of Figure 1A, for example, a second masking layer could be used to mask the passivation layers **33a** and **33d** while electroplating solder structures on the passivation layers metallurgy structures **34b** and **34c**. The masking layers could then be removed followed by removing the exposed portions of the under bump metallurgy layer to provide the structure of Figure 2A. Metallurgy structures according to the present

invention may be used with a full range of lead/tin solders and/or other tin based solders as well as other solders known to those of skill in the art.

A solder reflow operation can then be performed as shown in Figure 2B, such that solder is heated above its melting temperature. The reflow operation may cause passivation layers **33b'-c'** to react with the solder structures **35b'-c'**, and the passivation layers may diffuse into the solder structures. Solder may also diffuse into the barrier layers to provide first barrier layers **31b1'** and **31c1'** of the barrier material and diffused solder and second barrier layers **31b2'** and **31c2'** free of diffused solder. As further shown in Figure 2B, metallurgy structures **34a'** and **34d'** can be maintained free of solder for subsequent wire bonding. In addition, the solder surfaces may be cleaned after reflow.

A second integrated circuit substrate **41'** including pads **43b'** and **43c'** thereon may be provided for solder bonding to the first integrated circuit substrate **21'** using solder structures **35b'** and **35c'**. The second integrated circuit substrate may include input/output pads and a protective insulating layer similar to those of the first substrate. Moreover, the pads **43b'** and **43c'** may include metallurgy structures on input/output pads such that the pads **43b'** and **43c'** allow bonding to the solder structures **35b'** and **35c'**. As shown in Figure 2B, the second integrated circuit substrate **41'** including pads **43b'** and **43c'** may be brought into alignment with the solder structures **35b'** and **35c'**, and the pads **43b'** and **43c'** can then be brought into contact with the solder structures **35b'** and **35c'**.

As shown in Figure 2C, a second reflow operation (heating the solder above its melting temperature) can be performed to provide solder bonding between the first and second substrates **21'** and **41'**. Each solder structure **35b'** and **35c'** can thus provide electrical and mechanical coupling between the two substrates. The metallurgy structures **34a'** and **34d'** that are free of solder can be used to provide wire bonding for the respective input/output pads **23a'** and **23d'** as further illustrated in Figure 2C. In particular, the wires **51a'** and **51d'** can be bonded to the metallurgy structures **34a'** and **34d'** using wire bonding techniques known to those having skill in the art. Moreover, the order of bonding the second substrate and bonding the wires can be changed according to the present invention. For example, the second substrate can be

solder bonded to the first substrate followed by bonding the wires so that the alignment of the substrates is not hindered by the wires and so that the wire bonds are not subjected to the heat treatment used to reflow the solder. Alternately, the wires may be bonded followed by solder bonding the two substrates so that the wire bonding is not hindered by the presence of the second substrate.

Examples of alternate operations of providing wire and solder bonds to a structure according to Figure 1C are illustrated in Figures 3A-B. As shown in Figure 3A, the first integrated circuit substrate **21"** may include input/output pads **23a"-d"** and protective insulating layer **25"** as discussed above. As further discussed above, metallurgy structures **34a"-d"** can provide solder or wire bonds, and may, for example, include respective under bump metallurgy layers **29a"-d"**, barrier layers **31a"-d"**, and passivation layers **33a"-d"**. These structures can be provided, for example, as discussed above with regard to Figures 1A-C.

Solder structures **35b"** and **35c"**, however, may first be provided on pads **43b"** and **43c"** of second integrated circuit substrate **41"**. The solder structures may be provided on the second integrated circuit substrate using solder ball placement, electroplating, evaporation, or other techniques known to those having skill in the art. As shown in Figure 3A, the solder structures **35b"** and **35c"** on the pads **43b"** and **43c"** can be brought into alignment with the respective metallurgy structures **34b"-c"**.

As shown in Figure 3B, the solder structures **35b"** and **35c"** can then be brought into contact with the respective metallurgy structures **34b"-c"**, and a reflow operation performed to provide solder bonds between the first and second substrates. The reflow operation may cause passivation layers **33b"-c"** to react with the solder structures, and the passivation layers **33b"-c"** may diffuse into the respective solder structures **35b"-c"**. Solder may also diffuse into barrier layers **31b"-c"** to provide first barrier layers **31b1"** and **31c1"** of the barrier material and diffused solder and second barrier layers **31b2"** and **31c2"** free of diffused solder. As before, metallurgy structures **34a"** and **34d"** can be maintained free of solder for wire bonding.

As further shown in Figure 3C, wires **51a"** and **51d"** can be bonded to metallurgy structures **34a"** and **34d"** using techniques known to those having

skill in the art. While the wires are discussed as being bonded after solder bonding the second substrate to the first substrate, the wires could be bonded prior to bonding the first and second substrates.

As discussed above with regard to Figures 2A-C and 3A-B, two reflow operations can be used to solder bond the two substrates. Alternately, a single reflow operation can be used to bond the solder structures to both substrates at the same time. For example, solder balls can be placed, solder can be electroplated, or solder can be otherwise provided on one substrate; the substrates can be aligned and brought into contact; and a single reflow operation can be performed to bond the two substrates.

Structures and operations according to the present invention can thus be used to solder bond first and second substrates, and to provide wire bonds to one or both of the substrates. Because a metallurgy structure according to the present invention can be used to receive solder bonds or wire bonds, the same processing operations can be efficiently used to form metallurgy structures for both solder and wire bonding.

By way of example, a first substrate **121** may have a plurality of metallurgy structures **134a-d** wherein each of the metallurgy structures may accept either a solder bond or a wire bond as shown in Figure 4. Because all of the metallurgy structures have a shared structure, the metallurgy structures can be efficiently and simultaneously provided using the same processing operations. A second substrate **141**, including front and back sides **141a** and **141b**, may include pads **143b-c** adapted for solder bonding as shown in Figure 5. The pads **143b-c** may have structures similar to that of metallurgy structures **134a-d** or the pads may have other structures suitable for solder bonding.

The pads **143b-c** and the metallurgy structures **134b-c** have a mating arrangement such that the pads **143b-c** and the metallurgy structures **134b-c** can be aligned and solder bonded as shown in Figure 6. In particular, solder can be provided on pads **143b-c** and/or the metallurgy structures **134b-c**. The substrate **141** can then be "flipped" and aligned with the substrate **121**; the pads **143b-c** and the metallurgy structures **134b-c** can be brought into proximity with solder therebetween; and a reflow operation can be performed to bond the two substrates. Accordingly, the back side **141b** of the substrate

141 is visible in Figure 6 with the pads **143b-c** and the metallurgy structures **134b-c** between the first and second substrates **141** and **121**.

The metallurgy structures **134a** and **134d** are free of solder and can be used for bonding wires **151a** and **151d** as further shown in Figure 6. Accordingly, the two substrates **121** and **141** can be electrically and mechanically coupled using solder bonds between pads **143b-c** and metallurgy structures **134b-c**, and the substrate **121** can be electrically coupled with a next level packaging structure using wires **151a** and **151d**. The substrate **121**, for example, may be mechanically coupled to a next level packaging substrate such as a printed circuit board with electrical coupling being provided by the wires **151a** and **151d**.

Each of the various operations such as providing a first substrate including input/output pads, forming metallurgy structures, providing solder, bonding a second substrate to the first substrate, and bonding wires to the first substrate discussed above can be performed in one or more processing locations. For example, a chip fabrication facility may be used to provide the first substrate including the input/output pads, a bumping facility may be used to provide the metallurgy structures on the first substrate, and a packaging facility may be used to bond the first and second substrates and to bond wires. Moreover, one or more of these different facilities may be owned by different commercial entities.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.